

AMENDMENTS TO THE CLAIMS

Listing of Claims

Claim 1 (currently amended): A circuit comprising:

- 5 an operational amplifier comprising a positive input end, a negative input end, and
 an output end;
 a first input impedance coupled between the negative input end and a first input
 signal;
 a second input impedance coupled between the negative input end and a second
10 input signal; and
 a first output impedance coupled between the negative input end and the output
 end;
 wherein resistances of the first and second input impedances are controlled by a
 first and a second control signals respectively, so that the resistances of the
15 first and second input impedances are substantially different from each other
 and are close to each other.

- Claim 2 (currently amended): The circuit of claim 1 wherein [[resistances of the first
and second input impedances are close to each other]] the first input impedance
20 is a switched capacitor circuit, the switched capacitor circuit comprises:
 a capacitor coupled between a first node and a second node;
 a first switch with one end coupled to the first node and another end used as an
 end of the switched capacitor circuit;
 a second switch coupled between the first node and a common node;
25 a third switch with one end coupled to the second node and another end used as
 another end of the switched capacitor circuit; and
 a fourth switch coupled between the second node and the common node.

- Claim 3 (currently amended): The circuit of claim [[2]] 1 wherein the circuit has a
30 high input impedance characteristic.

Claim 4 (currently amended): The circuit of claim [[2]] 1 wherein the first output impedance is a resistive-impedance, the circuit has a high voltage attenuation characteristic.

5 Claim 5 (currently amended): The circuit of claim [[2]] 1 wherein the first output impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

10 Claim 6 (currently amended): The circuit of claim 1 wherein the first input impedance is a switched capacitor circuit, the switched capacitor circuit comprises:
a capacitor coupled between a first node and a [[ground end]] common node;
a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and
15 a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit,
wherein the first switch and the second switch are turned on alternately by the first control signal.

20 Claim 7 (previously presented): A circuit comprising:
a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;
a first input impedance coupled between the negative input end and a first input signal;
25 a second input impedance coupled between the positive input end and the first input signal;
a third input impedance coupled between the negative input end and a second input signal, the third input impedance being substantially equivalent to the second input impedance; and
30 a fourth input impedance coupled between the positive input end and the second input signal, the fourth input impedance being substantially equivalent to the first input impedance;

wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively.

5 Claim 8 (original): The circuit of claim 7 wherein resistances of the first and second input impedances are close to each other.

Claim 9 (original): The circuit of claim 8 wherein the circuit has a high input impedance characteristic.

10 Claim 10 (original): The circuit of claim 7 further comprising:
a first output impedance coupled between the negative input end and the positive output end; and
a second output impedance coupled between the positive input end and the negative output end.

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Claim 11 (original): The circuit of claim 10 wherein the first and the second output impedances are a resistive-impedance, the circuit has a high voltage attenuation characteristic.

20 Claim 12 (original): The circuit of claim 10 wherein at least one the first and the second output impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

25 Claim 13 (original): The circuit of claim 7 wherein the first input impedance is a switched capacitor circuit, the switched capacitor circuit comprises:
a capacitor coupled between a first node and a ground end;
a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and
a second switch with one end coupled to the first node and another end used as
30 another end of the switched capacitor circuit,
wherein the first switch and the second switch are turned on alternately by the first control signal.

Claim 14 (previously presented): A circuit comprising:

- a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;
- 5 a first input impedance coupled between the negative input end and a first input signal;
- a second input impedance coupled between the positive input end and a second input signal;
- 10 a first output impedance coupled between the negative input end and the positive output end;
- a second output impedance coupled between the negative input end and the negative output end;
- a third output impedance coupled between the positive input end and the positive output end, the third output impedance being substantially equivalent to the
- 15 second output impedance; and
- a fourth output impedance coupled between the positive input end and the negative output end, the fourth output impedance being substantially equivalent to the first output impedance,
- wherein resistances of the first and second output impedances are controlled by a
- 20 first and a second control signals respectively;
- wherein the resistances of the first and the second output impedances are close to each other.

Claim 15 (previously presented): The circuit of claim 14 wherein the resistances of the

25 first and the second output impedances are so controlled by the first and the second control signals as to be substantially different from each other.

Claim 16 (original): The circuit of claim 15 wherein the first and the second input

30 impedance is a resistive-impedance, the circuit has a high voltage gain characteristic.

Claim 17 (original): The circuit of claim 15 wherein at least one the first and the

second input impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

5 Claim 18 (original): The circuit of claim 14 wherein the first output impedance is a switched capacitor circuit, the switched capacitor circuit comprises:
a capacitor coupled between a first node and a ground end;
a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and
10 a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit,
wherein the first switch and the second switch are turned on alternately by the first control signal.

Claim 19 (previously presented): A circuit comprising:
15 a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;
a first input impedance coupled between the negative input end and a first input signal;
a second input impedance coupled between the positive input end and the first
20 input signal;
a third input impedance coupled between the negative input end and a second input signal, the third input impedance being substantially equivalent to the second input impedance;
a fourth input impedance coupled between the positive input end and the second
25 input signal, the fourth input impedance being substantially equivalent to the first input impedance;
a first output impedance coupled between the negative input end and the positive output end;
a second output impedance coupled between the negative input end and the
30 negative output end;
a third output impedance coupled between the positive input end and the positive output end, the third output impedance being substantially equivalent to the

second output impedance; and
a fourth output impedance coupled between the positive input end and the negative
output end, the fourth output impedance being substantially equivalent to the
first output impedance,
5 wherein the positive output end is for outputting a first output signal, and the
negative output end is for outputting a second output signal.

Claim 20 (previously presented): The circuit of claim 19 wherein the first input
impedance, the second input impedance, the third input impedance, the fourth
10 input impedance, the first output impedance, the second output impedance, the
third output impedance, or the fourth output impedance is a switched capacitor
circuit.

Claim 21 (previously presented): The circuit of claim 7 wherein the resistances of the
15 first and second input impedances are so controlled by the first and the second
control signals respectively, that they are substantially different from each other.